

### IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A communication channel comprising:

a link level protocol having an ~~input, an output~~ input/output, a driver line and a receiver line;

a driver connected to the driver line, wherein the driver includes a driver output, a driver circuit, and an impedance control circuit, wherein the impedance control circuit includes an impedance control output connected to the driver circuit, and wherein the impedance control circuit modifies a driver output signal as a function of an external signal;

a canceller/equalizer connected to the driver line and the driver output, wherein the canceller/equalizer includes ~~an~~ a canceller/equalizer output, and wherein the canceller/equalizer generates a receive signal as a function of data on the driver line and the driver output; and

a receiver connected to the receiver line and the canceller/equalizer output.

2. (Original) The communication channel of claim 1 wherein the external signal is the temperature of a resistive circuit.

3. (Currently Amended) A communication channel comprising:

a link level protocol having an ~~input, an output~~ input/output, a driver line and a receiver line;

a driver connected to the driver line, wherein the driver includes a driver output;

a canceller/equalizer connected to the driver line and the driver output, wherein the canceller/equalizer includes ~~an~~ a canceller/equalizer output, and wherein the canceller/equalizer generates a receive signal as a function of data on the driver line and the driver output; and

a receiver connected to the receiver line and the canceller/equalizer output, wherein the receiver includes a receiver circuit and a bit deskew circuit, wherein the bit deskew circuit deskews signals from the receiver circuit as a function of a clock signal.

4. (Previously Presented) The communication channel of claim 3 wherein the receiver further comprising a clock receiver, wherein the clock receiver has a clock receiver output connected to the bit deskew circuit, and wherein the clock receiver receives the clock signal and centers the clock.

5. (Currently Amended) A communication channel comprising:

a link level protocol having an ~~input, an output~~ input/output, a driver line and a receiver line;

a driver connected to the driver line, wherein the driver includes a driver output, a driver circuit, and an impedance control circuit, wherein the impedance control circuit includes an impedance control output connected to the driver circuit, and wherein the impedance control circuit modifies a driver output signal as a function of an external signal;

a canceller/equalizer connected to the driver line and the driver output, wherein the canceller/equalizer includes ~~an~~ a canceller/equalizer output, and wherein the canceller/equalizer generates a receive signal as a function of data on the driver line and the driver output; and

a receiver connected to the receiver line and the canceller/equalizer output, wherein the receiver includes a receiver circuit and a bit deskew circuit, wherein the bit deskew circuit deskews signals from the receiver circuit as a function of a clock signal.

6. (Original) The communication channel of claim 5 wherein the external signal is a voltage across a resistive circuit.

7. (Previously Presented) The communication channel of claim 5 wherein the receiver further comprising a clock receiver, wherein the clock receiver has a clock receiver output connected to the bit deskew circuit, and wherein the clock receiver receives the clock signal and centers the clock.

8. (Canceled)

9. (Canceled)

10. (Currently Amended) A communications system, comprising:

a communications medium;

a plurality of processors including a first and second processor, wherein each processor includes at least one processor line;

a first transceiver connected to the first processor and to the communications medium, wherein the first transceiver comprises a link level protocol, a driver including a driver output, a driver circuit and an impedance control circuit, a canceller/equalizer, and a receiver; and

a second transceiver connected to the second processor and to the communications medium, wherein the second processor communicates with the first processor over the communications medium;

wherein the link level protocol includes an ~~input, an output~~ input/output, a driver line and a receiver line;

wherein the driver is connected to the driver line, wherein the impedance control circuit includes an impedance control output connected to the driver circuit, and wherein the impedance control circuit modifies a driver output signal as a function of an external signal;

wherein the canceller/equalizer is connected to the driver line and the driver output, wherein the canceller/equalizer includes ~~an~~ a canceller/equalizer output, and wherein the canceller/equalizer generates a receive signal as a function of data on the driver line and the driver output; and

wherein the receiver is connected to the receiver line and the canceller/equalizer output.

11. (Previously Presented) The communications system of claim 10 wherein the external signal is based on temperature of a resistive circuit.

12. (Previously Presented) The communications system of claim 10 wherein the external signal is a function of a voltage across a resistive circuit.

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Currently Amended) A communications system comprising:

a communications medium;

a plurality of processors including a first and second processor, wherein each processor includes at least one processor line;

a first transceiver connected to the first processor and to the communications medium, wherein the first transceiver comprises a link level protocol, a driver including a driver output, a driver circuit and an impedance control circuit, a canceller/equalizer, and a receiver including a receiver circuit and a bit deskew circuit; and

a second transceiver connected to the second processor and to the communications medium, wherein the second processor communicates with the first processor over the communications medium;

wherein the link level protocol includes an ~~input, an output~~ input/output, a driver line and a receiver line;

wherein the driver is connected to the driver line, wherein the impedance control circuit includes an impedance control output connected to the driver circuit, and wherein the impedance control circuit modifies a driver output signal as a function of an external signal;

wherein the canceller/equalizer is connected to the driver line and the driver output, wherein the canceller/equalizer includes ~~an~~ a canceller/equalizer output, and wherein the canceller/equalizer generates a receive signal as a function of data on the driver line and the driver output; and

wherein the receiver is connected to the receiver line and the canceller/equalizer output, wherein the bit deskew circuit deskews signals from the receiver circuit as a function of a clock signal.

17. (Previously Presented) The communications system of claim 16 wherein the external signal is based on temperature of a resistive circuit.

18. (Previously Presented) The communications system of claim 16 wherein the receiver further comprising a clock receiver, wherein the clock receiver has a clock receiver output connected to the bit deskew circuit, and wherein the clock receiver receives the clock signal and centers the clock.

19. (Previously Presented) The communications system of claim 16 wherein the external signal is a function of a voltage across a resistive circuit.

20. (Currently Amended) A communications system, comprising:

a communications medium;

a processor with at least one processor line; and

a transceiver connected to the processor and to the communications medium, wherein the transceiver comprises a link level protocol, a driver including a driver output, a driver circuit and an impedance control circuit, a canceller/equalizer, and a receiver;

wherein the link level protocol includes ~~an input, an output~~ input/output, a driver line and a receiver line;

wherein the driver is connected to the driver line, wherein the impedance control circuit includes an impedance control output connected to the driver circuit, and wherein the impedance control circuit modifies a driver output signal as a function of an external signal;

wherein the canceller/equalizer is connected to the driver line and the driver output, wherein the canceller/equalizer includes ~~an~~ a canceller/equalizer output, and wherein the canceller/equalizer generates a receive signal as a function of data on the driver line and the driver output; and

wherein the receiver is connected to the receiver line and the canceller/equalizer output.

21. (Previously Presented) The communications system of claim 20 wherein the external signal is based on temperature of a resistive circuit.

22. (Previously Presented) The communications system of claim 20 wherein the external signal is a function of a voltage across a resistive circuit.

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Currently Amended) A communications system, comprising:

a communications medium;

a processor with at least one processor line; and

a transceiver connected to the processor and to the communications medium, wherein the transceiver comprises a link level protocol, a driver including a driver circuit and an impedance control circuit, a canceller/equalizer, and a receiver including a receiver circuit and a bit deskew circuit;

wherein the link level protocol includes an ~~input, an output~~ input/output, a driver line and a receiver line;

wherein the driver is connected to the driver line, wherein the impedance control circuit includes an impedance control output connected to the driver circuit, and wherein the impedance control circuit modifies a driver output signal as a function of an external signal;

wherein the canceller/equalizer is connected to the driver line and the driver output, wherein the canceller/equalizer includes ~~an~~ a canceller/equalizer output, and wherein the canceller/equalizer generates a receive signal as a function of data on the driver line and the driver output; and

wherein the receiver is connected to the receiver line and the canceller/equalizer output, wherein the bit deskew circuit deskews signals from the receiver circuit as a function of a clock signal.

27. (Previously Presented) The communications system of claim 26 wherein the external signal is based on temperature of a resistive circuit.

28. (Previously Presented) The communications system of claim 26 wherein the receiver further comprising a clock receiver, wherein the clock receiver has a clock receiver output connected to the bit deskew circuit, and wherein the clock receiver receives the clock signal and centers the clock.

29. (Previously Presented) The communications system of claim 26 wherein the external signal is a function of a voltage across a resistive circuit.

30. (New) The communication channel of claim 1, wherein the impedance control circuit increases voltage swing of the driver output signal to compensate for an increase in temperature at the driver.

31. (New) The communication channel of claim 5, wherein the impedance control circuit increases voltage swing of the driver output signal to compensate for an increase in temperature at the driver.

32. (New) The communications system of claim 10, wherein the impedance control circuit increases voltage swing of the driver output signal to compensate for an increase in temperature at the driver.

33. (New) The communications system of claim 16, wherein the impedance control circuit increases voltage swing of the driver output signal to compensate for an increase in temperature at the driver.

34. (New) The communications system of claim 20, wherein the impedance control circuit increases voltage swing of the driver output signal to compensate for an increase in temperature at the driver.

35. (New) The communications system of claim 26, wherein the impedance control circuit increases voltage swing of the driver output signal to compensate for an increase in temperature at the driver.